REMARKS

Claims 1-4, 6-14, and 16-22 were pending in this application.

Claims 1-4, 6-14, and 16-22 have been rejected.

Claims 7 and 17 have been amended as shown above.

Claims 1-4, 6-14, and 16-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-4, 6-14, and 16-22 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-4, 6-10, and 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,852 to Nakanishi ("*Nakanishi*") in view of U.S. Patent No. 6,167,501 to Barry et al. ("*Barry*"). The Office Action rejects Claims 11-14, 16-20, and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Nakanishi* and *Barry* in view of U.S. Patent No. 4,591,973 to Ferris, III et al. ("*Ferris*"). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce

evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

Claims 1 and 11 recite a "plurality of bypass tristate line drivers" having "output channels" coupled to a "common read data channel." Claims 1 and 11 also recite a "multiplexer" having a "first input channel coupled to [the] common read data channel" and an "output channel coupled to a first operand channel of a first execution unit."

The Office Action asserts that it would be obvious to modify the circuit of *Nakanishi* to

include the multiplexers of *Barry*. In particular, the Office Action asserts that it would be obvious to modify *Nakanishi* to include the multiplexers of *Barry* because the modification would "lower implementation costs." (*Office Action, Pages 3-4, Section 6*). The Office Action also asserts that it would be obvious to modify *Nakanishi* to include the multiplexers of *Barry* because "a multiplexer would be preferable to tri-state controls for buses." (*Office Action, Pages 13-14, Section 25*).

The Office Action fails to explain why a person skilled in the art would be motivated to either (i) replace some (but not all) of the tristate buffers T1-T72 in *Nakanishi* with the multiplexers of *Barry*, or (ii) insert a multiplexer of *Barry* between any of the buses 1-1 through 4-2 (the alleged "common read data channel") and any of the ALUs a1 through a4 (the alleged "execution unit") in *Nakanishi*.

Regarding the first scenario, the Office Action has merely provided a motivation to replace all of the tristate buffers T1-T72 in *Nakanishi* with the multiplexers of *Barry*. According to the Office Action, modifying *Nakanishi* to include the multiplexers of *Barry* may lower implementation costs, and a multiplexer may be preferable to tri-state controls for buses in certain instances. If anything, these motivations would cause someone skilled in the art to replace all of the tristate buffers T1-T72 in *Nakanishi* with multiplexers. However, Claims 1 and 11 are crystal clear – bypass circuitry includes both a "plurality of bypass tristate line drivers" and a "multiplexer." The Office Action fails to explain why someone skilled in the art would modify *Nakanishi* to replace only some of the tristate buffers T1-T72 with multiplexers while leaving others of the tristate buffers T1-T72 in place.

Regarding the second scenario, the Applicant has repeatedly noted that there is no need to place a multiplexer between any of the buses 1-1 through 4-2 and any of the ALUs a1 through a4. Each side of each ALU is coupled to a single one of the buses 1-1 through 4-2. For example, the left side of ALU a1 is coupled to bus 1-1, while the right side of ALU a1 is coupled to bus 1-2. Similarly, the left side of ALU a2 is coupled to bus 2-1, while the right side of ALU a2 is coupled to bus 2-2. There is no need to insert a multiplexer between the ALUs a1 through a4 and the buses 1-1 through 4-2 because each side of the ALUs already receives a single input from a single source.

At most, the Office Action has asserted that the tristate buffers T1-T72 in *Nakanishi* may be replaced by the multiplexers of *Barry*. In other words, the circuit of *Nakanishi* may be modified to remove all of the tristate buffers T1-T72 and insert the multiplexers of *Barry*. In contrast, Claims 1 and 11 recite "bypass circuitry" that includes both a "plurality of bypass tristate line drivers" and a "multiplexer." The Office Action fails to explain why someone skilled in the art would modify *Nakanishi* to replace some (but not all) of the tristate buffers T1-T72 with multiplexers.

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1 and 11 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-4, 6-14, and 16-22.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in

condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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